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EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 11/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,010	NIESEN, JOSEPH W.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/6/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-17 are presented for examination.

Information Disclosure Statement

The references listed in the information disclosure statements (IDS) submitted February 06, 2004 were considered. The submission is in compliance with the provisions of 37 CFR 1.97. The PTO-1449 form is attached.

Oath/Declaration

The Oath filed February 06, 2004 complies with all the requirements set forth in MPEP 602 and therefore is accepted.

Drawings

The drawings submitted February 06, 2004 are accepted.

Specification

The specification is object to because:

- It is noted throughout the specification Applicant uses "cyclic redundancy check" when infact it is "cyclic redundancy check code". It is understood that "code" could be "coding" as well.

Appropriate correction is requested.

Claim Objections

Claim 1 is objected to because of the following informalities:

- In line 3, the phrase, "...cyclic redundancy check..." needs to be replaced with "...cyclic redundancy check code..." The Examiner will interpret as such.

Appropriate correction is required.

Claim 2 is objected to because of the following informalities:

- In line 6, the phrase, "...cyclic redundancy check..." needs to be replaced with "...cyclic redundancy check code..." The Examiner will interpret as such.

Appropriate correction is required.

Claim 8 is objected to because of the following informalities:

- In line 2, the phrase, "...cyclic redundancy check..." needs to be replaced with "...cyclic redundancy check code..." The Examiner will interpret as such.

Appropriate correction is required.

Claim 10 is objected to because of the following informalities:

- In line 4, the phrase, "...cyclic redundancy check..." needs to be replaced with "...cyclic redundancy check code..." The Examiner will interpret as such.

Appropriate correction is required.

Claim 17 is objected to because of the following informalities:

- In line 3 and further in claim, the phrase, "...cyclic redundancy check..." needs to be replaced with "...cyclic redundancy check code..." The Examiner will interpret as such.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- The claim recites, "...stand-alone data packets..." which is not clear. "Stand-alone," as defined in The Authoritative Dictionary of IEEE Standards Terms 7th ed., means:

  "Pertaining to hardware or software that is capable of performing its function without being connected to other component; for example, a stand-alone word processing system."

  Therefore, it is not clear how "data packets" can be described as 'stand-alone" when they are always used in conjunction with something else for practical all uses. For the purposes of examination "stand-alone" will be disregarded.

Appropriate correction/clarification is requested.

Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- The claim recites, "...said data packets comprise multiple data packets" which is not clear since "data packets" is plural and multiple is plural as well. It is not clear how claim 7 further limits the parent claim and how multiple data packets is different from data packets. For the purposes of examination, the Examiner will make interpretations in accordance with MPEP 2111.

Appropriate correction is requested.

Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- The claim recites, "...to determine whether said at least one data packet was received by said receiver in substantially the same condition as transmitted..." which is not clear. The term substantially is a relative term and therefore it is not clear from the claim or the specification on how it is defined. Furthermore, it is noted that calculating the CRC at the receiver and comparing it with the received CRC will clearly determine if an error(s) exists, not the amount of errors. For the purposes of examination, the term "substantially" will be disregarded and the Examiner will make interpretations in accordance with MPEP 2111.

Appropriate correction is requested.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-15, 17-19 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Jedwab (USPN 5778013).

As per claim 1, Jedwab teaches a method for verifying the validity of transmitted digital information data bits arranged in one or more data packets (i.e., col. 6, lines 59-61) comprising: performing a cyclic redundancy check on said one or more data packets to obtain a check sequence for each said one or more data packets (i.e., col. 2, lines 24-26 and col. 6, line 65—col. 7, lines 1-6); and condensing said check sequence into a single reduced bit count check sequence equivalent (i.e., col. 2, lines 27-29 and col. 7, lines 7-12); and wherein the number of bits occupied by said reduced bit count check sequence equivalent is fewer than the number of bits occupied by said check sequences, thus freeing additional data bits for use by digital information data bits. The Examiner would like to point out that the number of bits (data + the CRC verification value) occupied by combining the partial CRC values would inherently free additional space since the all the partial CRCs are replaced with one CRC. Furthermore, it is noted that the limitation, "...the number of bits occupied by said reduced bit count check sequence equivalent is fewer than the number of bits occupied by said check sequences, thus freeing additional data bits for use by digital information data bits" is an effect of combining the partial CRC values.

As per claim 2, Jedwab teaches (i.e., col. 2, lines 22-23) transmitting said reduced bit count check sequence equivalent and said data packets; receiving said reduced bit count check sequence equivalent and said data packets; performing said cyclic redundancy check on said received data packets to obtain received check sequence; and comparing said reduced bit count received check sequence with said reduced bit count transmitted sequence to determine if said data packets were transmitted accurately (i.e., col. 2, lines 30-51). The Examiner would like to point out that Jedwab teaches that once the partial CRC values are combined to form a CRC verification value, the data and the one CRC verification value are transmitted across a communication medium and the one CRC verification value is used to determine if any errors are present (particularly, col. 2, lines 39-41).

As per claim 4, Jedwab teaches said condensing step is performed by an error correction code (i.e., col. 3, lines 65—col. 4, lines 1-6). The Examiner would like to point out that CRC coding is well known in the art as an error correction code. For example, see USPN 5007055, col. 4, lines 16-10.

As per claim 5, Jedwab teaches said data packets comprise multiple data packets within a superframe (i.e., col. 1, lines 53-58 and col. 2, lines 21-24). The Examiner would like to point out that a relatively "large" plurality of sub-blocks, for which partial CRC values are combined, may be easily constituted as superframe, since by definition a superframe only need to have 193 bit positions.

As per claim 6, Jedwab teaches said data packets comprise stand-alone data packets (i.e., col. 2, lines 53-58). See rejections under 35 USC 112.

As per claim 7, Jedwab teaches said data packets comprise multiple data packets (i.e., col. 2, lines 53-58). See rejections under 35 USC 112.

As per claim 8, Jedwab teaches a data transmission system (i.e., col. 2, lines 22-24) comprising: a transmitter operable to perform a cyclic redundancy check on at least one data packet to produce at least one check sequence representing said data packet (i.e., col. 2, lines 24-27); and a condensing device operable to condense said at least one check sequence into a check sequence equivalent that is smaller than said at least one check sequence (i.e., col. 2, lines 28-30); and wherein said at least one data packet and said check sequence equivalent are transmitted by said transmitter (i.e., col. 2, lines 23-24). The Examiner would like to point out that a "communications medium" inherently is a part of a transmitting device and a receiving device.

As per claim 9, Jedwab teaches the number of bits occupied by said check sequence equivalent is fewer than a number of bits occupied by said at least one check sequence, thus freeing additional data bits for use as information bits (i.e., col. 2, lines 27-31). The Examiner would like to point out that the act of combining the partial CRC values taught by Jedwab inherently would reduce the size and free additional data bit for information, since multiple CRC values are being recalculated and replaced by one CRC verification value (i.e., col. 2, lines 32-49).

As per claim 10, Jedwab teaches a receiving device (i.e., col. 2, lines 21-23) operable to receive said transmitted data packet and said transmitted check sequence equivalent and operable to perform cyclic redundancy check on said transmitted data packet (i.e., col. 2, lines 38-41).

As per claim 11, Jedwab teaches said receiving device comprising a forward error correction code to reduce transmitted data packets into single reduced bit count received CRC

sequence (i.e., col. 2, lines 38-42). The Examiner would like to point out that verification CRC value is recalculated on the data at the receiver and compared with the transmitted verification CRC value to determine if an error has occurred in the data. As previously stated, CRC coding is well known in the art as an error correction code. For example, see USPN 5007055, col. 4, lines 16-10.

As per claim 12, Jedwab teaches said receiving device comprising a comparator for comparing CRC sequence with said reduced bit count transmitted CRC sequence to determine if an error exists (i.e., col. 2, lines 38-42). The Examiner would like to point out that verification CRC values is recalculated on the data at the receiver and compared with the transmitted verification CRC value to determine if an error has occurred in the data.

As per claim 13, Jedwab teaches said condensing step is performed by an forward error correction code (i.e., col. 3, lines 65—col. 4, lines 1-6). The Examiner would like to point out that CRC coding is well known in the art as an forward error correction code. For example, see USPN 5007055, col. 4, lines 16-10.

As per claim 14, Jedwab teaches said condensing step is performed by an forward error correction code (i.e., col. 3, lines 65—col. 4, lines 1-6). The Examiner would like to point out that CRC coding is well known in the art as an forward error correction code which is implemented as a block code since the CRC value is determined based on blocks of data. For example, see USPN 5007055, col. 4, lines 16-10.

As per claim 15, Jedwab teaches said data packets comprise multiple data packets within a superframe (i.e., col. 1, lines 53-58 and col. 2, lines 21-24). The Examiner would like to point out that a relatively "large" plurality of sub-blocks, for which partial CRC values are combined,

may be easily constituted as superframe, since by definition a superframe only need to have 193 bit positions.

As per claim 17, Jedwab teaches a method for verifying the validity of transmitted digital information data bits arranged in one or more data packets (i.e., col. 6, lines 59-61) comprising: performing a cyclic redundancy check on said one or more data packets to obtain a check sequence for each said one or more data packets (i.e., col. 2, lines 24-26 and col. 6, line 65—col. 7, lines 1-6); and condensing said check sequence into a single reduced bit count check sequence equivalent (i.e., col. 2, lines 27-29 and col. 7, lines 7-12); and wherein the number of bits occupied by said reduced bit count check sequence equivalent is fewer than the number of bits occupied by said check sequences, thus freeing additional data bits for use by digital information data bits. The Examiner would like to point out that the number of bits (data + the CRC verification value) occupied by combining the partial CRC values would inherently free additional space since the all the partial CRCs are replaced with one CRC. Furthermore, it is noted that the limitation, "...the number of bits occupied by said reduced bit count check sequence equivalent is fewer than the number of bits occupied by said check sequences, thus freeing additional data bits for use by digital information data bits" is an effect of combining the partial CRC values. Jedwab also teaches (i.e., col. 2, lines 22-23) transmitting said reduced bit count check sequence equivalent and said data packets; receiving said reduced bit count check sequence equivalent and said data packets; performing said cyclic redundancy check on said received data packets to obtain received check sequence; and comparing said reduced bit count received check sequence with said reduced bit count transmitted sequence to determine if said data packets were transmitted accurately (i.e., col. 2, lines 30-51). The Examiner would like to

point out that Jedwab teaches that once the partial CRC values are combined to form a CRC verification value, the data and the one CRC verification value are transmitted across a communication medium and the one CRC verification value is used to determine if any errors are present (particularly, col. 2, lines 39-41).

As per claim 18, Jedwab teaches said condensing step is performed by an forward error correction code (i.e., col. 3, lines 65—col. 4, lines 1-6). The Examiner would like to point out that CRC coding is well known in the art as an forward error correction code. For example, see USPN 5007055, col. 4, lines 16-10.

As per claim 19, Jedwab teaches said data packets comprise multiple data packets within a superframe (i.e., col. 1, lines 53-58 and col. 2, lines 21-24). The Examiner would like to point out that a relatively "large" plurality of sub-blocks, for which partial CRC values are combined, may be easily constituted as superframe, since by definition a superframe only need to have 193 bit positions.

As per claim 21, Jedwab teaches identifying said data packets that are transmitted with errors so that said data packets with errors can be further processed (i.e., col. 2, lines 38-41). The Examiner would like to point out that the CRC verification value is used at the receiving end of the communication system to detect errors that may occur in the data.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3, 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jedwab (USPN 5778013) further in view of Isono et al. (Herein after: Isono, USPN 5007055).

As per claim 3, Jedwab does not explicitly teach to retransmit any of said packets that are received with errors as stated in the present application.

However, Isono substantially teaches, in an analogous art and in view of above rejections to claim 1, (i.e., Figure 5 and col. 3, line 57—col. 4, lines 1-10) the error correction code calculation circuit 12 produces an error correction code, such as a cyclic redundancy code (CRC), for each data block No. 1 to No. m, of, for example, 2 K Byte, which is a unit of transmission of the distribution information. The group of error correction codes produced, consisting of the error correction codes ECC-1, ECC-2, . . . ECC-m regarding all of the produced data blocks No. 1, No. 2, . . . No. m, is stored in the error correction code group holding storage 13. Particularly, Isono teaches (i.e., col. 6, lines 35-39) to retransmit any of said packets that are received with errors. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of retransmitting any of said packets that are received with errors within the teachings of Jedwab. This modification would have been obvious to one of ordinary skill in the art because one of ordinary in the art would have recognized that by retransmitting any data packets that are received with errors would be an efficient way of recovering for data loss especially when the corrupted data is received with large amounts of errors which may be beyond recovery otherwise.

As per claim 16, Jedwab does not explicitly teach to retransmit any of said packets that are received in a condition different then transmitted as stated in the present application.

However, Isono substantially teaches, in an analogous art and in view of above rejections to claim 8, (i.e., Figure 5 and col. 3, line 57—col. 4, lines 1-10) the error correction code calculation circuit 12 produces an error correction code, such as a cyclic redundancy code (CRC), for each data block No. 1 to No. m, of, for example, 2 K Byte, which is a unit of transmission of the distribution information. The group of error correction codes produced, consisting of the error correction codes ECC-1, ECC-2, . . . ECC-m regarding all of the produced data blocks No. 1, No. 2, . . . No. m, is stored in the error correction code group holding storage 13. Particularly, Isono teaches (i.e., col. 6, lines 35-39) to retransmit any of said packets that are received in a condition different then transmitted. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of retransmitting any of said packets that are received in a condition different then transmitted within the teachings of Jedwab. This modification would have been obvious to one of ordinary skill in the art because one of ordinary in the art would have recognized that by retransmitting any data packets that are received in a condition different then transmitted would be an efficient way of recovering for data loss especially when the corrupted data is received with large amounts of errors which may be beyond recovery otherwise.

As per claim 20, Jedwab does not explicitly teach to retransmit any of said packets that are received with errors as stated in the present application.

However, Isono substantially teaches, in an analogous art and in view of above rejections to claim 17, (i.e., Figure 5 and col. 3, line 57—col. 4, lines 1-10) the error correction code

calculation circuit 12 produces an error correction code, such as a cyclic redundancy code (CRC), for each data block No. 1 to No. m, of, for example, 2 K Byte, which is a unit of transmission of the distribution information. The group of error correction codes produced, consisting of the error correction codes ECC-1, ECC-2, . . . ECC-m regarding all of the produced data blocks No. 1, No. 2, . . . No. m, is stored in the error correction code group holding storage 13. Particularly, Isono teaches (i.e., col. 6, lines 35-39) to retransmit any of said packets that are received with errors. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of retransmitting any of said packets that are received with errors within the teachings of Jedwab. This modification would have been obvious to one of ordinary skill in the art because one of ordinary in the art would have recognized that by retransmitting any data packets that are received with errors would be an efficient way of recovering for data loss especially when the corrupted data is received with large amounts of errors which may be beyond recovery otherwise.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts are included herein for Applicant's review. For example:

Apisdorf teaches a system and method for checking for data transmission errors in a network includes a cyclic redundancy code (CRC) generator and a processing device. The CRC generator receives a stream of data representing cells in a packet of data. The CRC generator generates a CRC value for each cell and transmits the CRC value to a processing device. The processing device combines the cell CRC values to generate a CRC for a packet of data. The processing device then compares the packet CRC to an expected value to determine whether an error occurred in the data transmission.

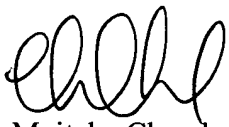
Higginson et al. teach a system wherein a packet is originated in a unit 10 as a data field DATA 11 plus a CRC (cyclic redundancy check) check field CRC 12 by a CRC circuit 13. This packet has a header HDR (with a routing information field RIF) added to it in a unit 20, converting it into a message for transmission through a message network. A check correction field CCF is computed by unit 23 in unit 20, by looking up precomputed check subfields stored with the routing subfields (the routing information field being constructed by selecting from the stored subfields), such that the CRC field is a valid CRC check field for the complete message. At the destination, unit 30 can be the final user unit, checking the entire message and extracting the data field DATA therefrom; the DATA field does not need to be checked, as the CRC field acts as a check both for the data field DATA alone and the entire message. (Alternatively, the message can be checked by a final switching unit 30 using a standard CRC check circuit 32 (and

similarly at intermediate units 30', 30") and the original packet can be checked by another standard CRC check circuit 42 in the final user unit 40.)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Mujtaba Chaudry
Art Unit 2133
November 13, 2006